


MIT
Wireless Gigabit Local Area Network
WiGLAN

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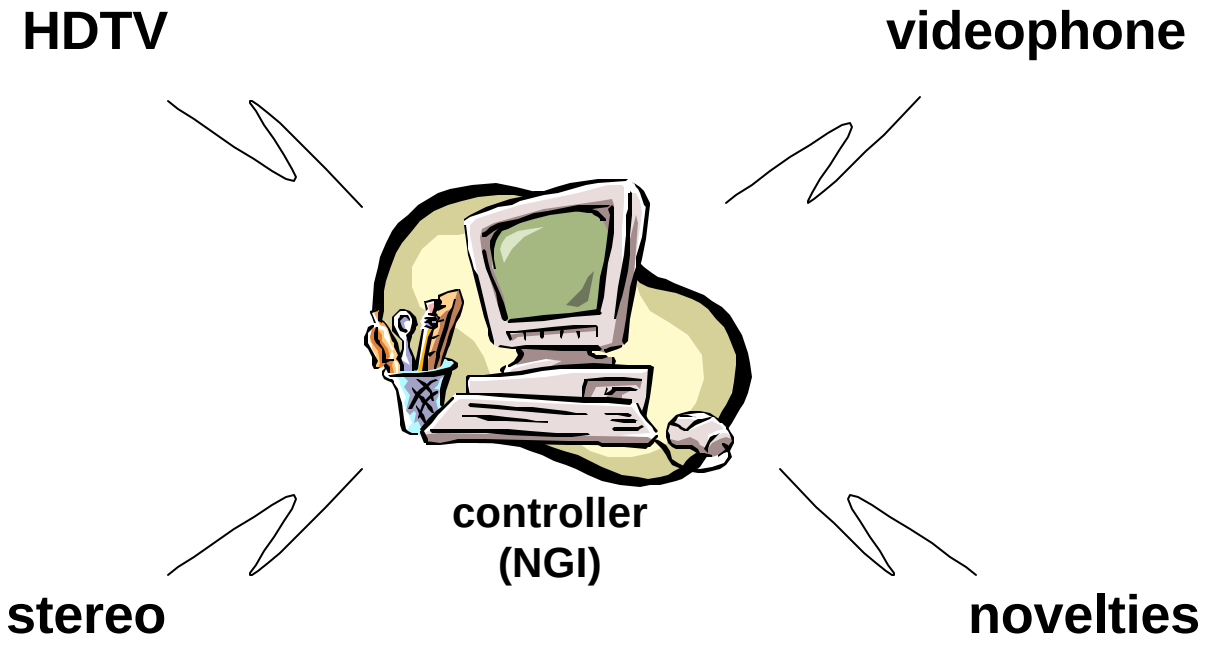
Sponsors: MARCO, SRC, MIT CICS

Wireless Gigabit Local Area Network (WiGLAN)

- PC Peripherals
- Consumer Electronics
- Interactive Video

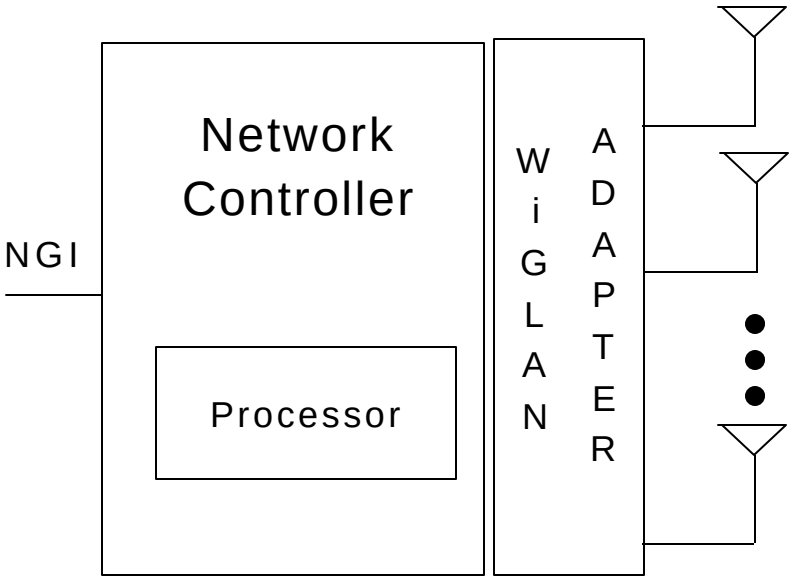


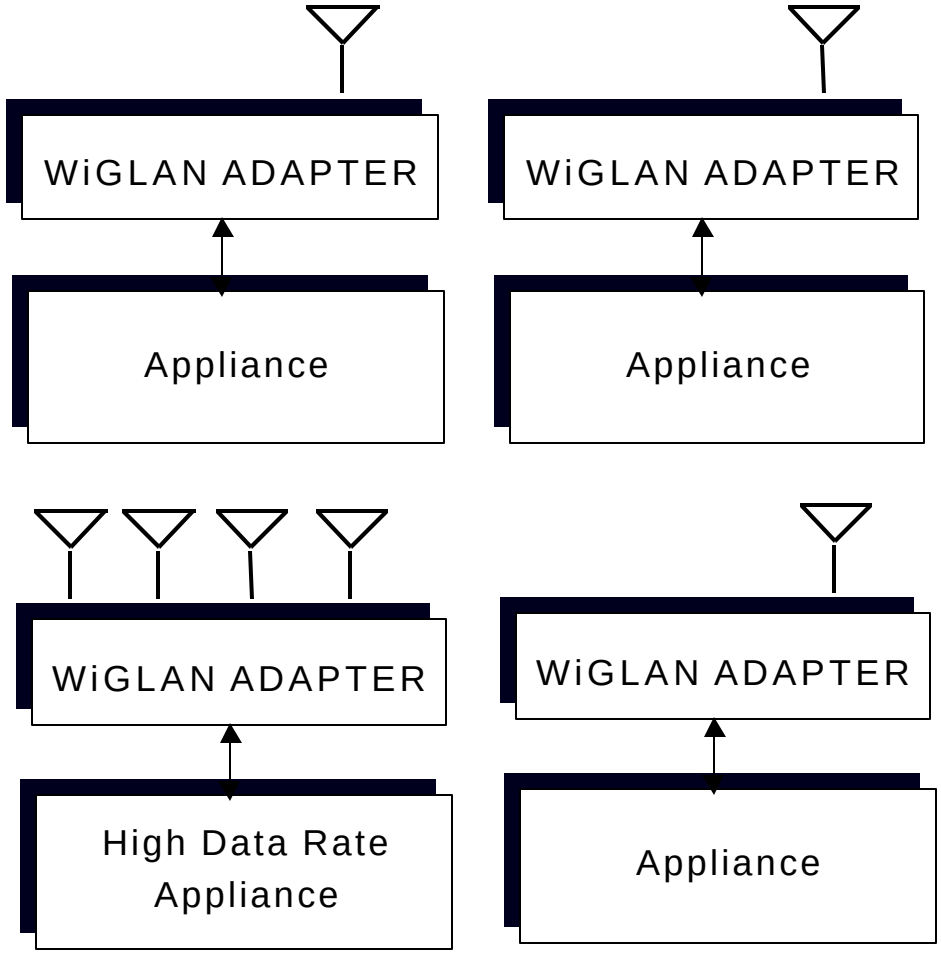
Research Goals

- **Demonstrate key circuit and system concepts to advance wireless LAN to** Gb/sec data rates
- Adaptive system **architecture to support wide range of data rates and quality of service**
- **Develop** low power design techniques **at the circuit, chip architecture and system level to support portable appliances**

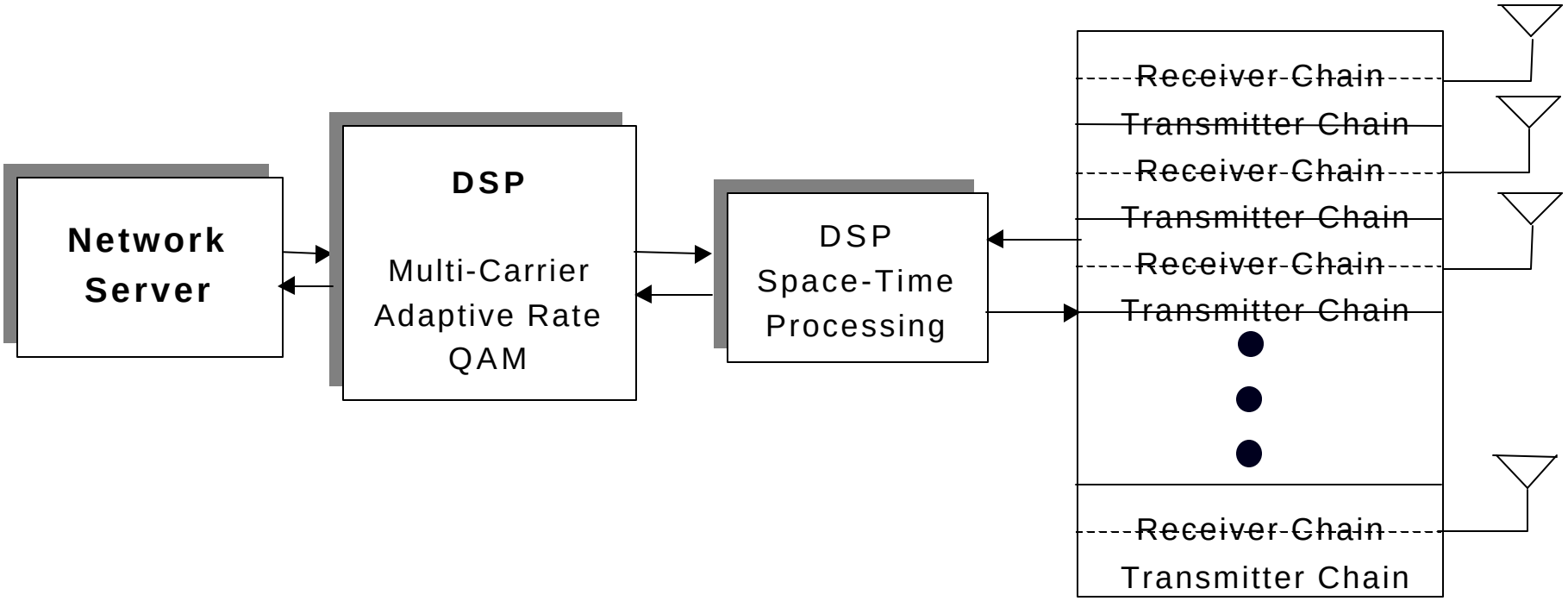
WiGLAN Architecture

- Network Controller
  - Allocates channels
  - Measures SNR
  - Space-Time Diversity





Network Controller with Space-Time Diversity

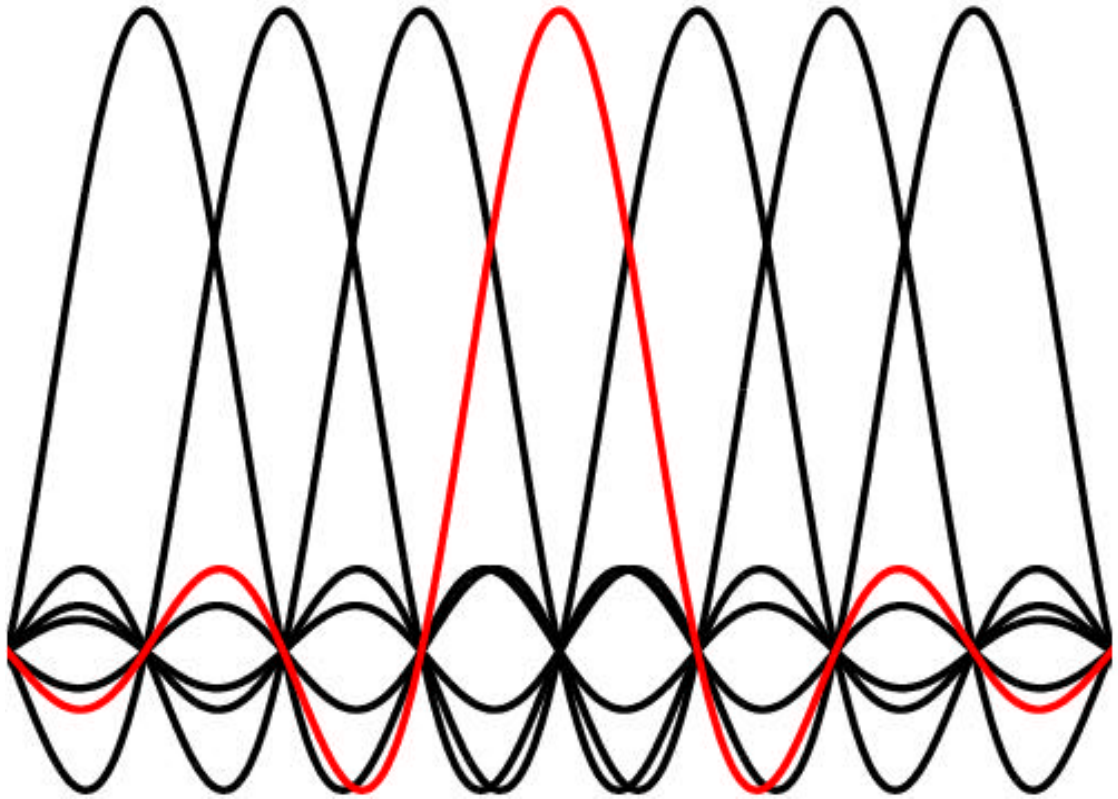


- **Digital Modulation**
- **Digital Space-Time Diversity Processing**
  - **Improves channel capacity**
- **Replicated Transmit/Receive Chain**

OFDM

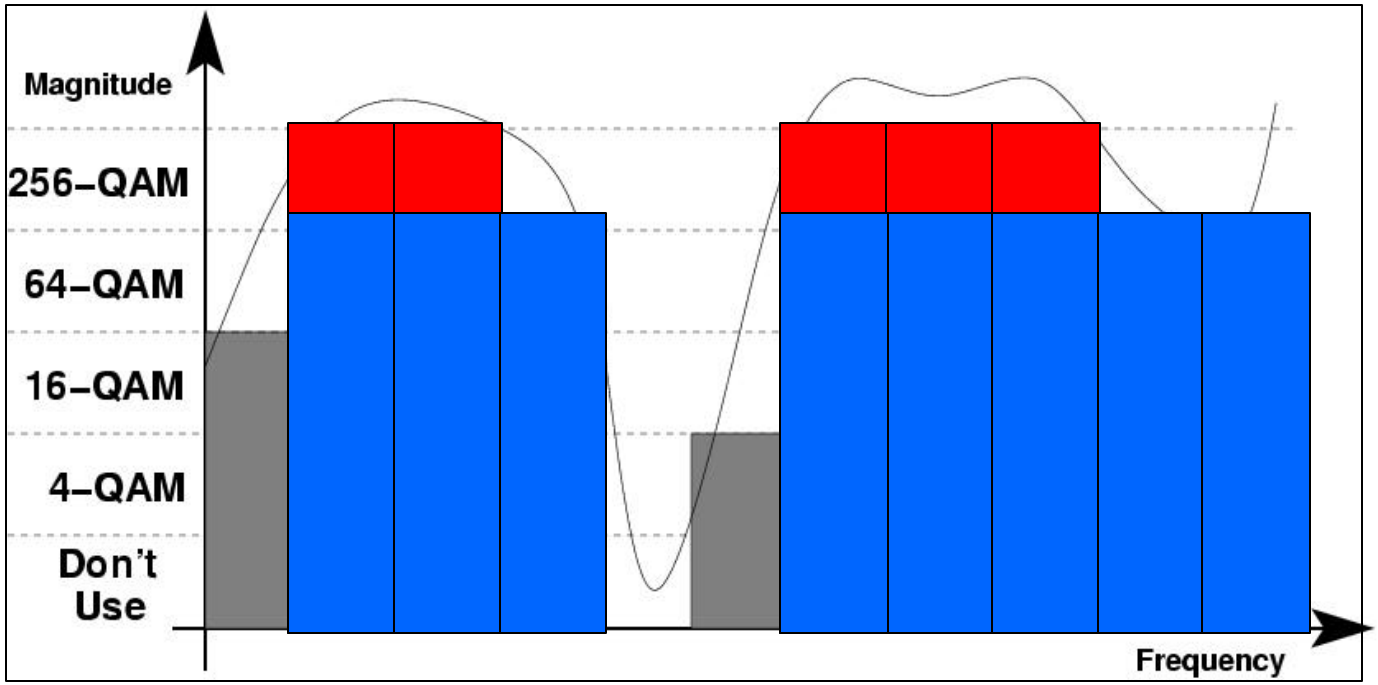
150 MHz bandwidth available in 5.8 GHz band, with bins ~1 MHz wide

- Conversion between time and frequency via (I)FFT
- Narrow bins provide more granularity for changing data demands
- Narrow bins increase total complexity, but allow greater potential for parallelism
- Cyclic prefix similar to frequency guard bands



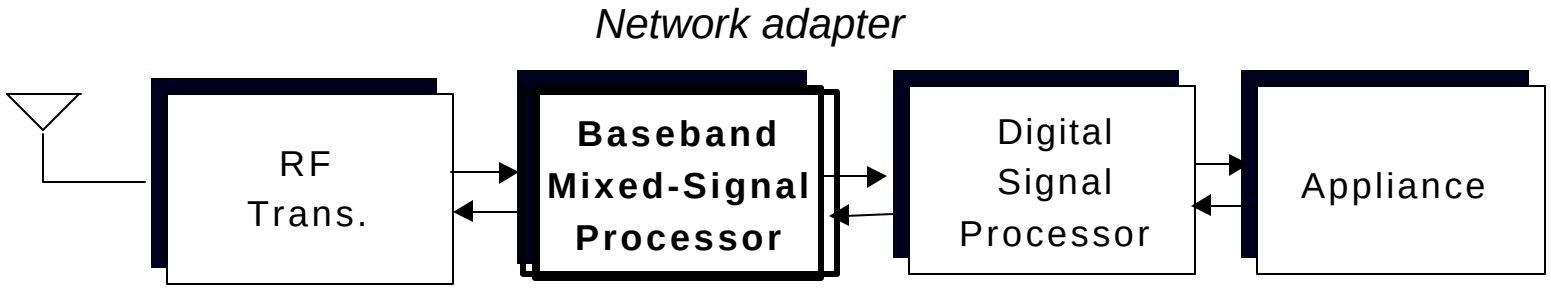
Adaptive Modulation

- Can adaptively change modulation for each bin based on measured channel response. Either optimal (gray) or coarse (dark gray) water pouring can be used.
- Most of the benefit comes from avoiding very bad frequency bins.



- Optimal: 54 b/s/Hz
- Coarse: All equal
  - 40 b/s/Hz
  - 48 b/s/Hz (best)
- Threshold may differ for each block
- Coarse requires less overhead to identify bin modulation

Network Adapter Block Diagram



- **Physically Small - Requires High Integration**
- **3 Major IC's - RF, Baseband Mixed Signal, DSP**
- **Quality of Service - Scaleable with Power Dissipation**

Baseband Mixed-Signal Processor

Wideband A/D Conversion

- DC-150MHz, oversampled at 600MSPS
- ~12 bit linearity/resolution
- Low power (~1W, core)

Programmable Gain Amplifier

- 0-20dB, 72 dB Linearity

Channel Equalization

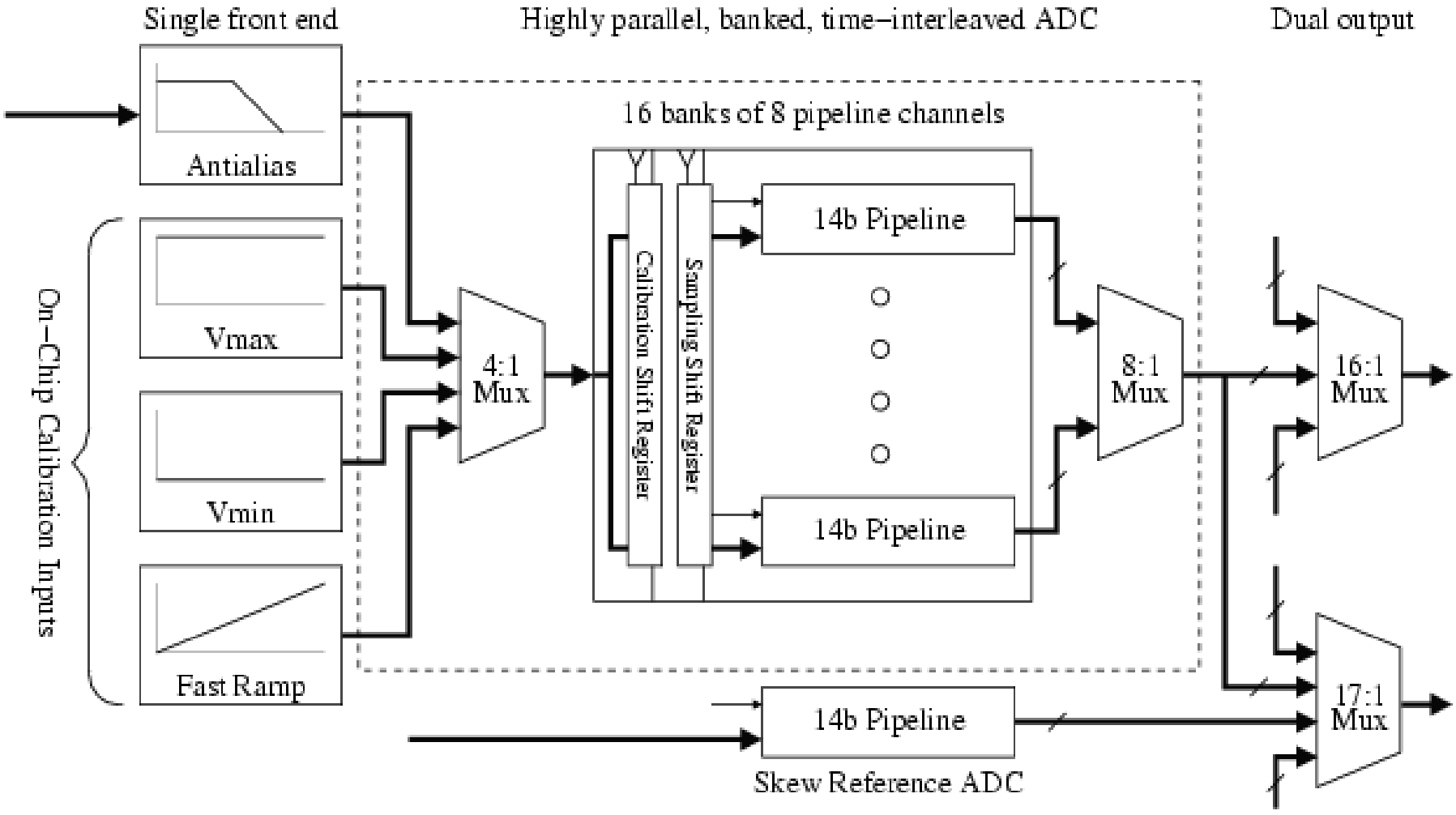
- Channel fading characteristic requires only modest amplitude equalization

Proposed ADC Architecture

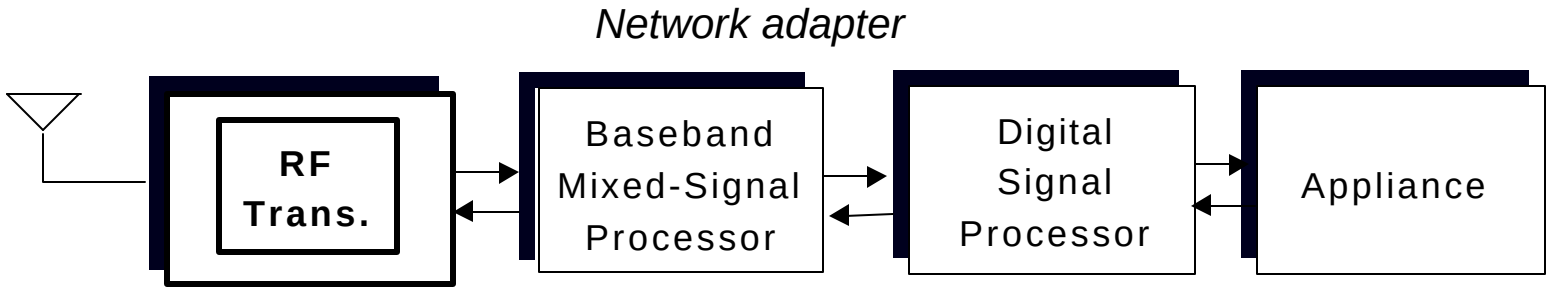
Highly parallel array of time-interleaved ADCs

- 16 banks of 8 14-bit pipeline ADCs, each running at approximately 5MHz
- 2x oversampling at 600 MHz effective sampling rate
- Continuous background digital calibration of gain, offset, and inter-channel timing skew and input path mismatch errors
- Novel token-passing control scheme to reduce clock interconnect
- Back-end cubic interpolation to resample the output data stream and cancel timing skew

Proposed Architecture, Cont'd



Network Adapter Block Diagram



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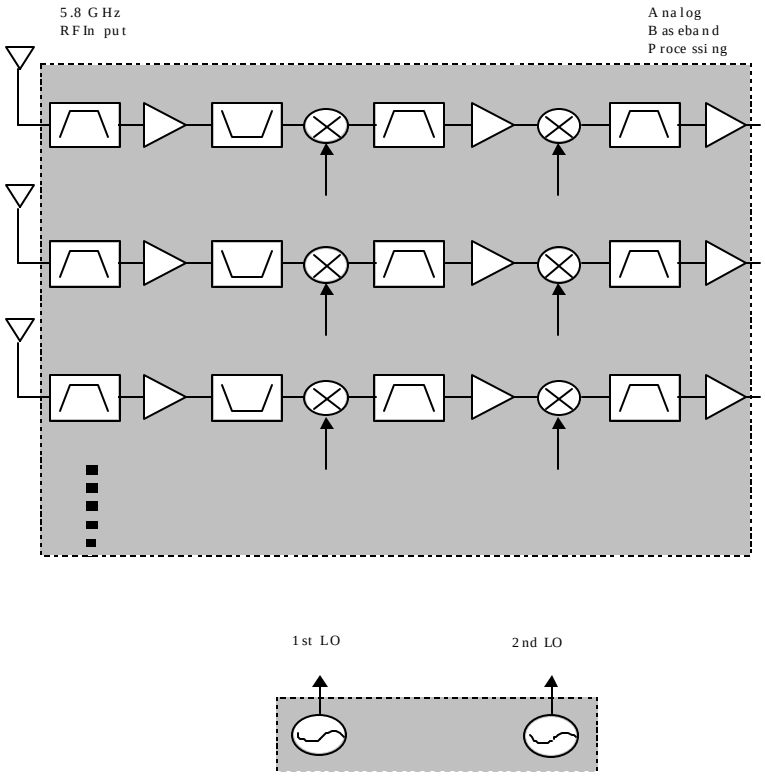
WiGLAN Receiver: Architectural Approach



Primary Goals

- Multiple receivers in parallel
- Fully integrated analog front end

Major Challenges

- Design & implementation of wide-bandwidth high frequency filters
- Isolation between receivers

WiGLAN Receiver: Integrated Filters

Motivations:

Isolation & matching complexities with use of multiple external discrete filters

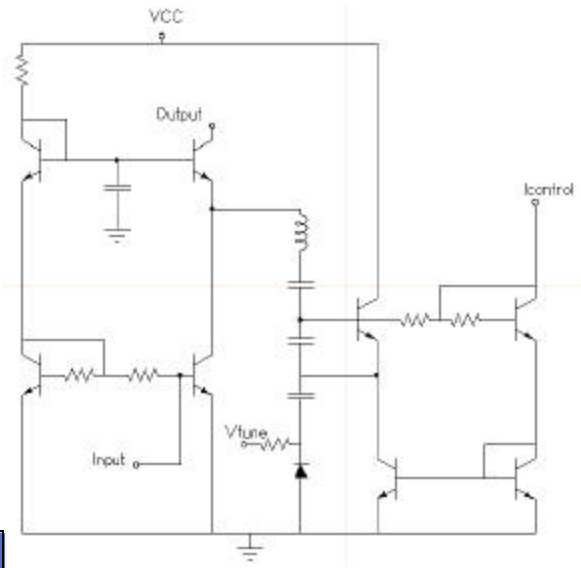
Approaches:

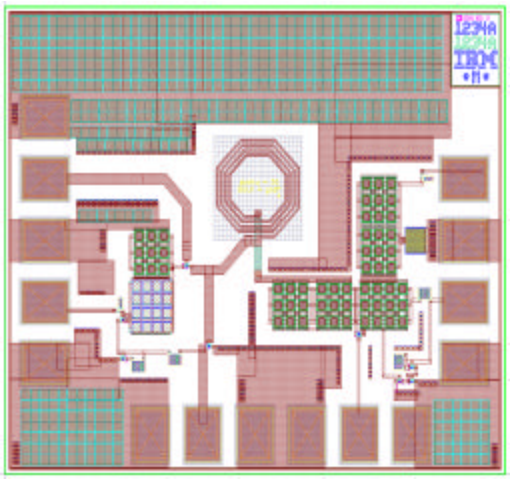
- Q-enhancement techniques to compensate low Q on-chip inductors
- Simple & novel filter building blocks
- Traditional passive & active integrated circuit techniques reuse, where appropriate, to implement higher order filters

Challenges:

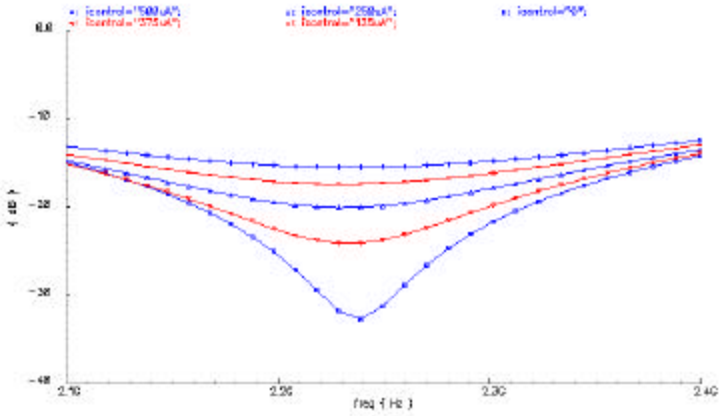
- Filter stability with component tolerances
- Receiver linearity and noise degradation

WiGLAN Receiver: Image Reject Filter
(Prototype Building Block)

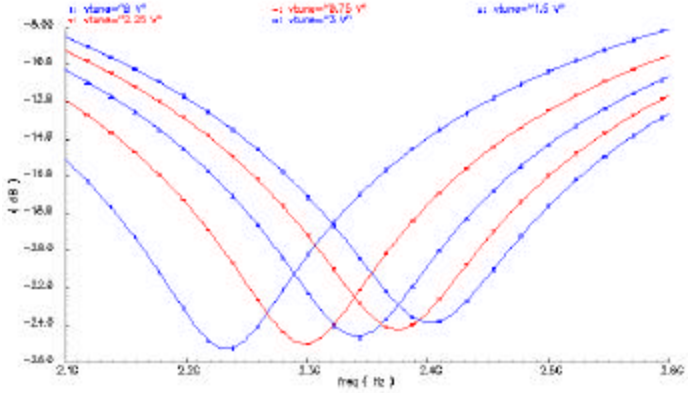




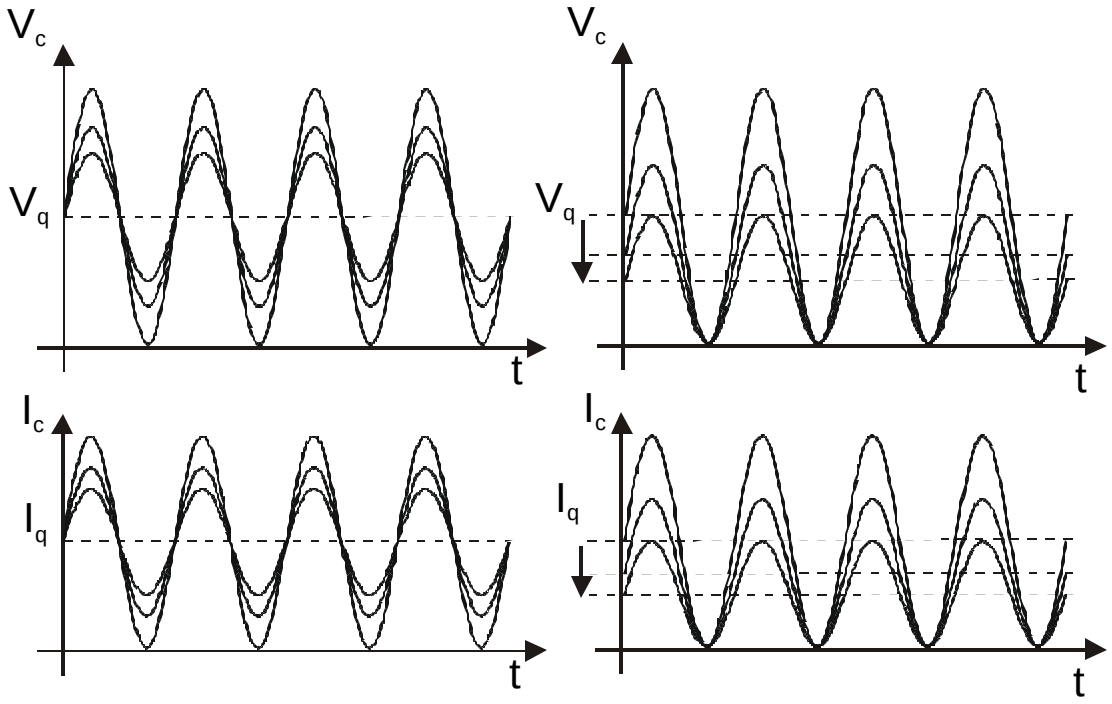
Tunable rejection response



Tunable center frequency



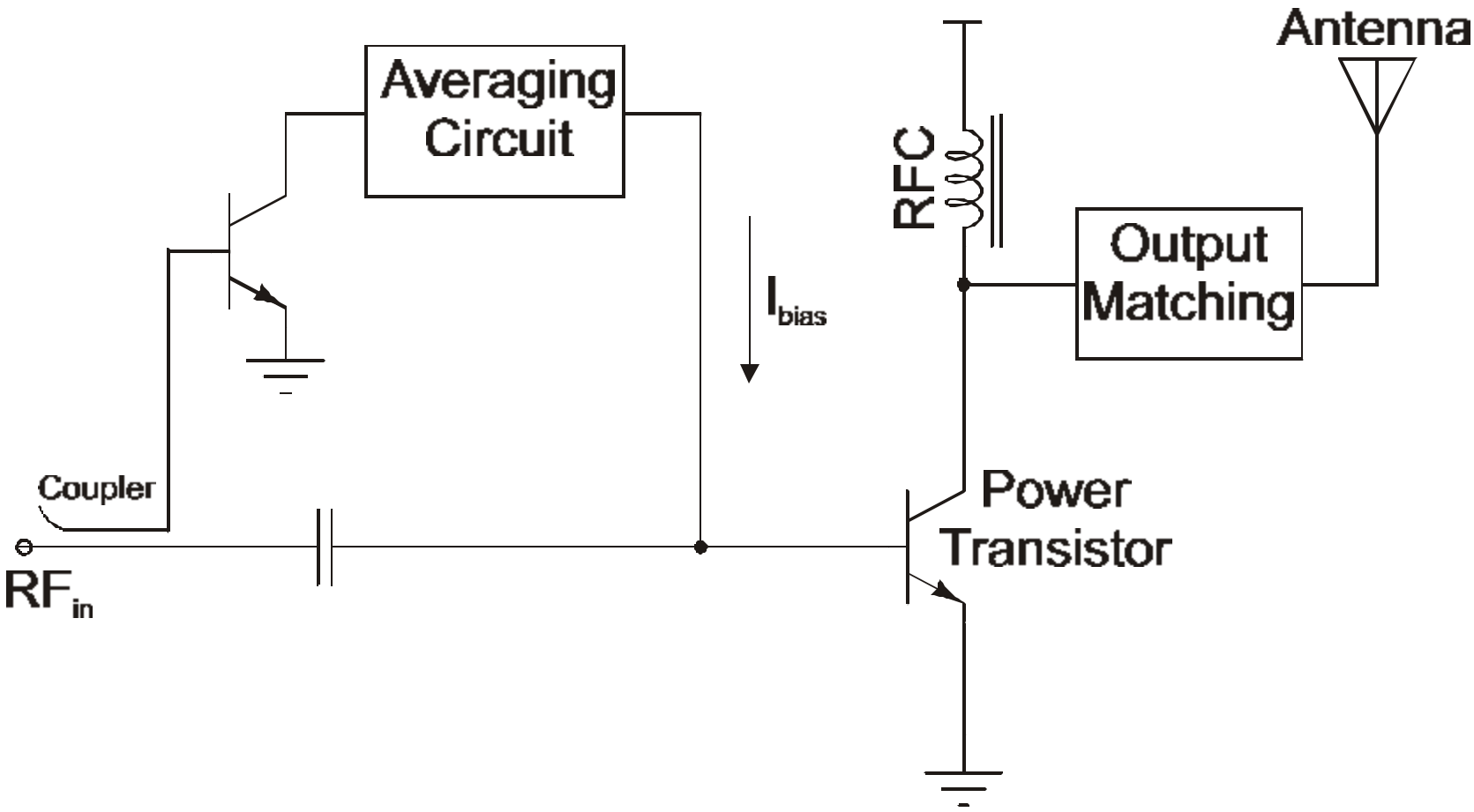
Power Amplifier Efficiency



To improve efficiency at low power:

- ***Adapt the biasing current***, or
- Adapt the supply voltage, or
- Adapt both current and voltage

Adaptive biasing – Concepts



Adapt the bias current based on power level

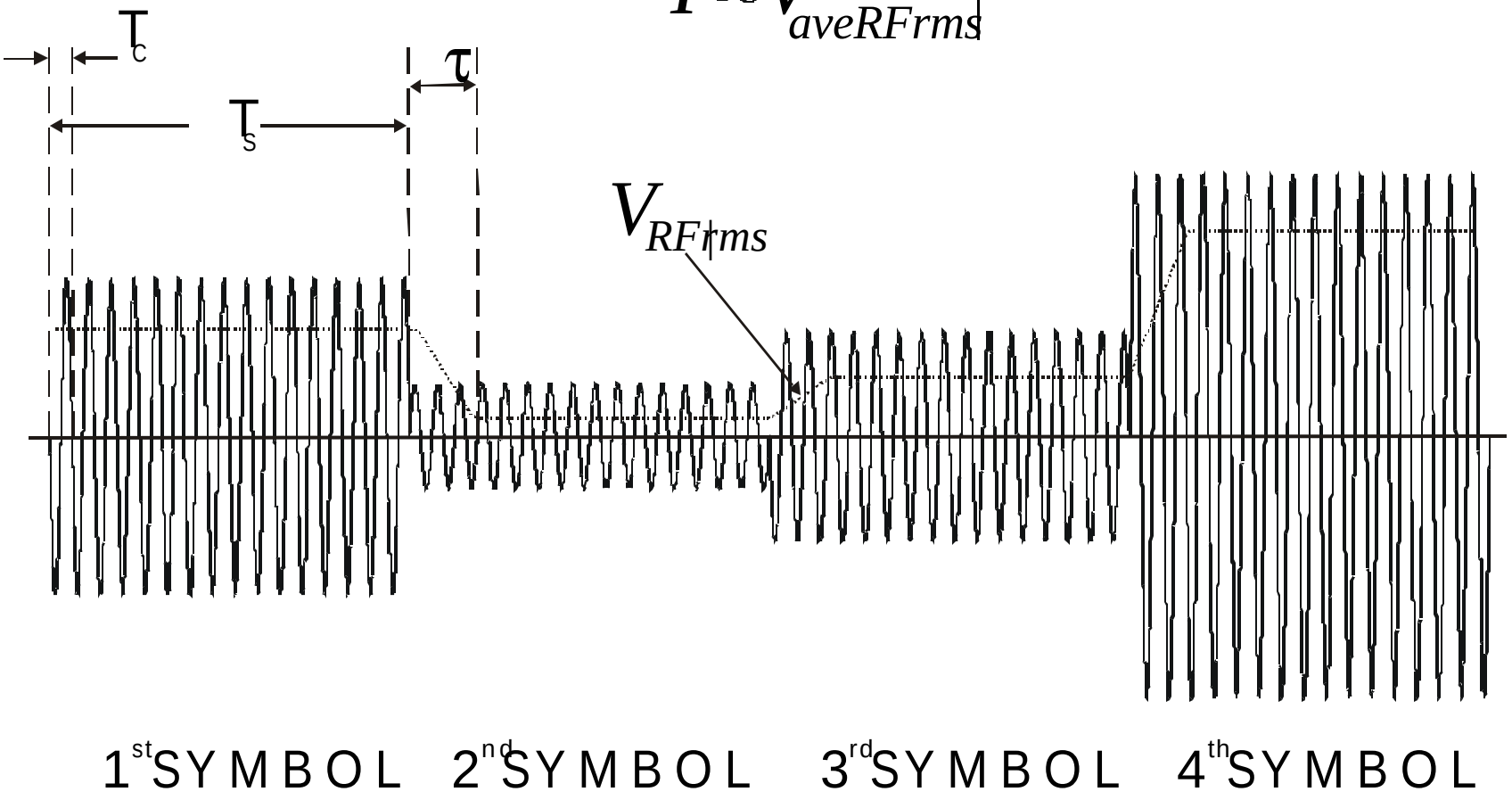
⇨ Improve efficiency at lower power levels

The Averaging Circuit

τ ave. circuit time constant
T_C carrier period
T_S QAM symbol period

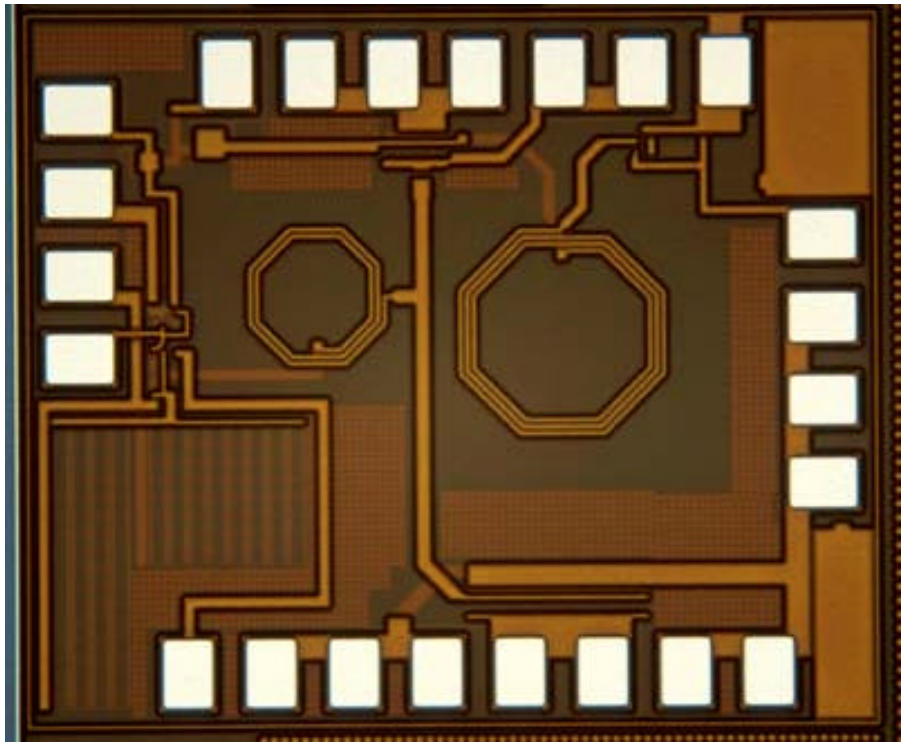
$$T_C << t = RC << T_S$$

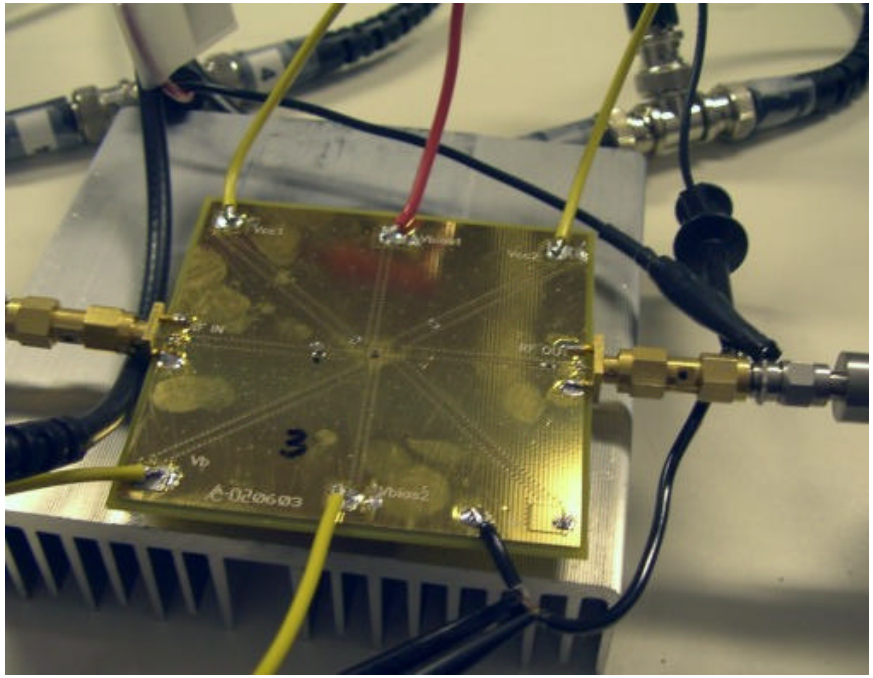
$$I \propto V_{aveRFrms}$$



Die Photo and Test Board

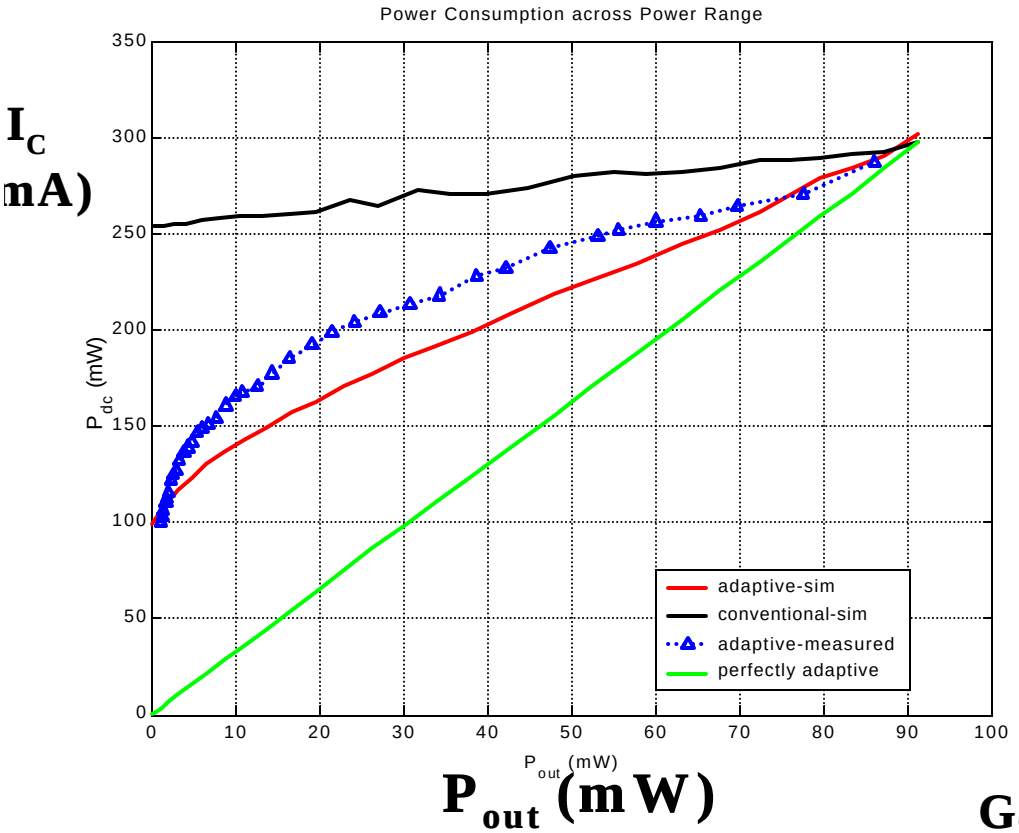
Chip Dimension: 1.05mm x 1.25mm
IBM 7HP SiGe BiCMOS



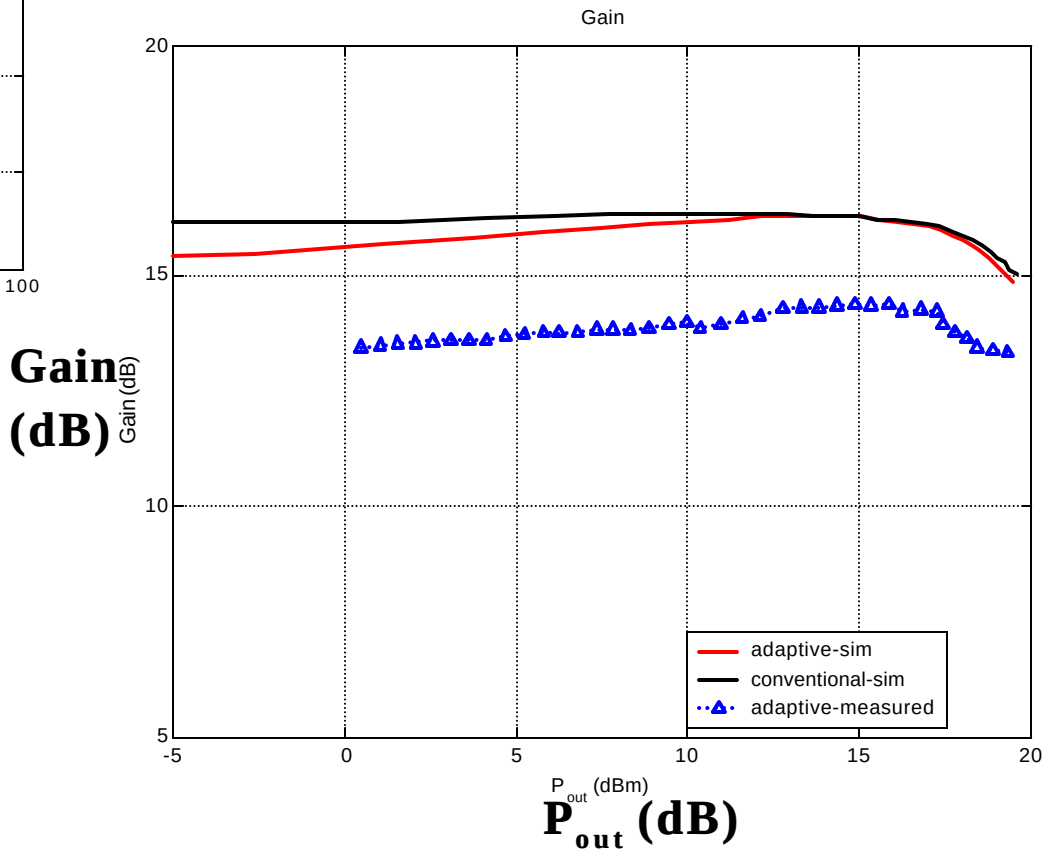


The chip is mounted directly on board to minimize lead inductance

Adaptive biasing – Results



Gain remains nearly constant during adaptation



Adaptation saves up to 2.5X power

Summary

Wireless Gigabit LAN

Provides a Research Platform for

High Data Rate/Low Power Circuit Design

- **DSP.**
- **Baseband Analog**
- **RFIC**

That can be applied to a variety of applications